REMARKS

The foregoing claim amendment amends claims 5 and 14. Now in the application are Claims 1-20 of which Claims 1, 10, and 19 are independent. The following remarks address all stated grounds for rejection, and Applicants respectfully submit that the presently pending claims, as identified above, are in condition for allowance.

Claims Being Objected To

Claims 5 and 14 are objected to because of minor informalities. In the foregoing claim amendments, Applicants have amended claims 5 and 14 to remove the informalities. In light of the foregoing claim amendments, Applicants request the Examiner to reconsider and withdraw the objection to claims 5 and 14.

Claims Being Rejected Under 35 U.S.C. § 102

Claims 1-3, 5-8, 10-12 and 14-19 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,758,112 ("Yeager"). Applicants respectfully traverse this rejection for the following reasons.

Claim 1 is directed to a method for managing a number of physical registers using a first structure, a second structure and a third structure. The first structure holds information identifying available physical registers that are free to be assigned as a destination operand for instructions. A physical register assignment is stored in the second structure noting that a selected physical registers is assigned as a destination operand for the architectural register of a selected instruction. The physical register assignment of the selected physical register is transferred from the second structure to the third structure after retirement of the selected instruction. Information identifying the selected physical register as available is transferred from the third structure to the first structure *when the architectural register is assigned as a destination operand for a subsequent instruction.* Claim 10 is another method claim reciting similar limitations, and claim 19 is a system claim that parallels claim 1.

Applicants submit that Yeager fails to disclose that *when the architectural register is assigned as a destination operand for a subsequent instruction, information identifying the*

selected physical register as available is transferred from the third structure to the first structure, as recited in claim 1. The Examiner asserts in the Office Action that the free list, the mapping table and the active list disclosed in Yeager correspond to the first structure, the second structure and the third structure of the claimed invention, respectively. Applicants respectfully disagree.

Yeager discloses register renaming for the execution of instructions in a processor. In Yeager, each of the mapping tables (204, 206) maps a logical register number into a corresponding physical register number. See Yeager, Fig. 1 and column 8, lines 27-33. The active list (212) contains an ordered list of all active instructions that have been *decoded*. The instructions remain active until the instructions complete in program order or are aborted by reversed branch decision or an exception. See Yeager, column 15, lines 39-43.

Fig. 2 of the Yeager reference describes the execution of ADD instruction (250). The logical register number (256) is appended to the active list (212). The free list (210) forwards the physical register number (272) to the mapping table (206). The mapping table (206) outputs an old physical destination (282) associated with the logical register number (256) to the active list (212). The active list (212) also includes the done bit (286), which indicates whether the instruction (276) completes. The old physical destination (282) returns to the free list (210) *when the instruction (276) completes or graduates*.

In contrast, the claimed invention transfers information identifying the selected physical register as available from the third structure to the first structure *when the architectural register is assigned as a destination operand for a subsequent instruction*. In the Yeager reference, the old physical destination returns from the active list to the free list *when a subsequent instruction completes or graduates*. The Yeager reference does <u>not</u> disclose that the old physical destination returns from the active list to the free list when the logical register is assigned as a destination operand for a subsequent instruction. In Yeager, when the logical register is assigned as a destination operand for a subsequent instruction, the old physical destination is appended from the mapping table to the active list.

With the arrangement described above, the claimed invention may provide memory structures for efficient tracking and recycling of physical register assignments. The claimed

invention can reduce the size of the memory structures needed to track the usage of physical registers and the recycling of these registers.

In light of the arguments set forth above, Applicants submit that the Yeager reference fails to disclose each and every element of claims 1, 10 and 19. Applicants therefore request the Examiner to reconsider and withdraw the rejection of Claims 1-3, 5-8, 10-12 and 14-19 under 35 U.S.C. §102(b).

Claims Being Rejected Under 35 U.S.C. § 103

Claims 4, 13 and 20 are rejected under 35 U.S.C. § 103(a) as unpatentable over Yeager. Applicants respectfully traverse the rejection for the following reasons.

Claim 4, 13 and 20 depend on independent claims 1, 10 and 19, respectively. Applicants submit that Yeager fails to teach that *when the architectural register is assigned as a destination operand for a subsequent instruction, information identifying the selected physical register as available is transferred from the third structure to the first structure*, as recited in claims 1, 10 and 19. Claim 4, 13 and 20, which depend on independent claims 1, 10 and 19, respectively, are not rendered obvious over the cited prior art reference. Applicants therefore request the Examiner to reconsider and withdraw the rejection of Claims 4, 13 and 20 under 35 U.S.C. §103(a).

Claims Being Rejected Under 35 U.S.C. § 103

Claims 9 and 18 are rejected under 35 U.S.C. § 103(a) as unpatentable over Yeager in view of Tanebaum, Structured Computer Organization, 2nd Edition, 1984, page 11 ("Tanebaum"). Applicants respectfully traverse the rejection for the following reasons.

Claim 9 and 18 depend on independent claims and 10, respectively. Tanebaum is cited by the Examiner to provide teachings for the subject matter added in claims 9 and 18, which relates to software performing the method recited in claims 1 and 10. Tanebaum, however, does not teach that *when the architectural register is assigned as a destination operand for a subsequent instruction, information identifying the selected physical register as available is transferred from the third structure to the first structure*, as recited in claims 1 and 10. In light

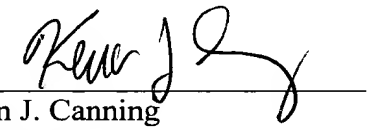
of the arguments set forth above, Applicants submit that the Yeager and Tanebaum references fail to teach or suggest all of the limitations of independent claims 1 and 10. Claim 9 and 18, which depend on independent claims 1 and 10, respectively, are not rendered obvious over the cited prior art references. Applicants therefore request the Examiner to reconsider and withdraw the rejection of Claims 9 and 18 under 35 U.S.C. §103(a).

Conclusion

In view of the remarks set forth above, Applicant contends that Claims 1-20 are presently pending in this application, are patentable and in condition for allowance. If the Examiner deems there are any remaining issues, we invite the Examiner to call the undersigned at (617) 227-7400.

Dated: August 15, 2005

Respectfully submitted,

By 

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